Electronic Version
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[LOW LEAKAGE MONOTONIC CMOS LOGIC]

Abstract

A low leakage monotonic CMOS logic circuit and a method, a method of design and a system for designing such circuits. The circuit, including: one or more logic stages, at least one of the logic stages having a predominantly high input state or having a predominantly low input state; wherein the logic stages having the predominantly high input state, comprise one or more thin gate dielectric and high threshold voltage PFETs with respect to a reference PFET and one or more thick gate dielectric and low threshold voltage NFETs with respect to a reference NFET; and wherein the logic stages having the predominantly low input state, comprise one or more thick gate dielectric and low threshold voltage PFETs with respect to the reference PFET and one or more thin gate dielectric and high threshold voltage NFETs with respect to the reference NFET.